

altairTM 8800b

TECHNICAL INFORMATION

The ALTAIR 8800b computer is a general purpose byte-oriented machine (8-bit word). It uses a common 100-pin bus structure that allows for expansion of either standard or custom plug-in modules. It supports up to 64K of directly addressable memory and can address 256 separate input and output devices. The ALTAIR 8800b computer has 78 basic machine language instructions and is comprised of a power supply board, an interface board, a central processing unit (CPU) board, and a display/control board.

Power Supply Board

The Power Supply Board provides two output voltages to the ALTAIR 8800b computer bus, a positive and negative 18 volts. It includes a bridge rectifier circuit and associated filter circuit, a 10-pin terminal block connector, and the regulating transistors for the positive and negative 18 volt supplies.

Interface Board

The Interface Board buffers all signals between the display/control board and the ALTAIR 8800b bus. It also contains eight parallel data lines which transfer data to the CPU from the Display/Control board.

CPU Board

The CPU board controls and processes all instruction data within the ALTAIR 8800b computer. It contains the model 8080A microprocessor circuit, the master timing circuit, eight input and eight output data lines to the ALTAIR bus, and control circuits.

Display/Control Board

The Display/Control Board conditions all ALTAIR 8800b front panel switches and receives information to be displayed on the front panel. It contains a programmable read only memory (PROM), switch and display control circuits, and control circuits to condition the CPU.

NEW DESIGN FEATURES

Several new design features have been incorporated into the electronic and mechanical areas of the ALTAIR 8800b computer. Some of the new design features include additional front panel capabilities, redesigned power supply, and various electronic and mechanical design advancements.

New Front Panel Switches

Five new front panel switch positions have been added to the ALTAIR 8800b computer to expand the front panel capability.

1. SLOW position: Permits execution of a program at a rate of approximately 2 machine cycles per second or slower. The normal machine speed is approximately 500,000 machine cycles per second. The ALTAIR 8800b operates in the slow mode as long as the SLOW switch is depressed on the front panel.
2. DISPLAY ACCUMULATOR position: Displays the contents of the CPU accumulator register on the ALTAIR 8800b front panel.
3. LOAD ACCUMULATOR position: Loads the information present on the lower eight front panel address switches into the CPU accumulator register.
4. INPUT ACCUMULATOR position: Inputs the information present at an Input/Output device into the CPU accumulator register. The Input/Output device is selected on the upper eight front panel address switches.
5. OUTPUT ACCUMULATOR position: Outputs the contents of the CPU accumulator register to a selected input/output device. The input/output device is selected on the upper eight front panel address switches.



New Power Supply

The new power supply in the ALTAIR 8800b contains an 8 volt, 18 ampere tapped secondary supply which permits the addition of up to 16 printed circuit cards, and pre-regulated positive and negative 18 volt, 2-ampere supplies. A multiple tapped primary transformer provides for 110/220 volt operation and a 50/60 Hz operation.

Electronic Design Advancements

The electronic design advancements on the ALTAIR 8800b are in the CPU and front panel circuit boards.

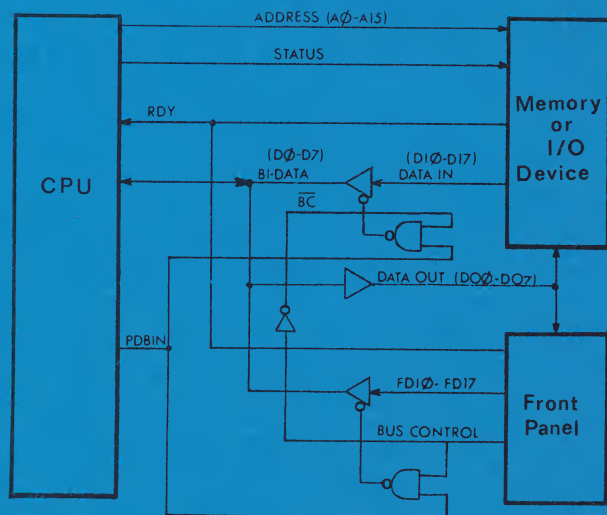
1. CPU. The new CPU circuit board uses the Intel 8224 clock generator integrated circuit (IC). The 8224 IC provides a specified clock frequency to the ALTAIR 8800b using an external crystal and dividing the crystal frequency down to 2MHz. Therefore, both the clock pulse widths and phasing (as well as frequency) are crystal controlled.
2. Front Panel. All front panel data lines are connected to an interface which buffers them from the rest of the ALTAIR 8800b. The front panel circuits also use a programmable read only memory (PROM) which contains programs for the following eight functions:
EXAMINE
EXAMINE NEXT
ACCUMULATOR DISPLAY
ACCUMULATOR LOAD
DEPOSIT
DEPOSIT NEXT
INPUT ACCUMULATOR
OUTPUT ACCUMULATOR

The front panel circuits also have a wiring option which allows the CPU to perform a complete instruction cycle or a single machine cycle during the single step or slow operation.

Mechanical Design Advancements

The mechanical design advancements on the ALTAIR 8800b are incorporated for ease of assembly and maintenance.

1. The wiring harness connection which exists on the front panel of the ALTAIR 8800 is replaced with ribbon cables. These ribbon cables connect the front panel circuits to the interface circuits.
2. The four slot expander cards in the ALTAIR 8800 have been replaced by a single piece 18-slot motherboard. The 18-slot motherboard contains 100 solder lands which comprise the 100 pin bus.
3. A new multi-color and redesigned dress panel is used in the ALTAIR 8800b. The front surface of the dress panel has a protective sheet of mylar to insure that the graphics are not rubbed or scratched off.



8800b BLOCK DIAGRAM

8800b BLOCK DIAGRAM DESCRIPTION

The 8800b computer contains four main circuits: a Central Processing Unit (CPU), a Memory, an Input/Output (I/O), and a Front Panel. The CPU controls the interpretation and execution of software instructions, and the Memory stores the software information to be used by the CPU. The I/O provides a communication link between the CPU and external device. The Front Panel allows the operator to manually perform various operations with the 8800b. The 8800b block diagram description explains: A) the communication between the CPU and the memory or I/O circuits; and B) the communication between the CPU and the front panel.

CPU to Memory or I/O Operation

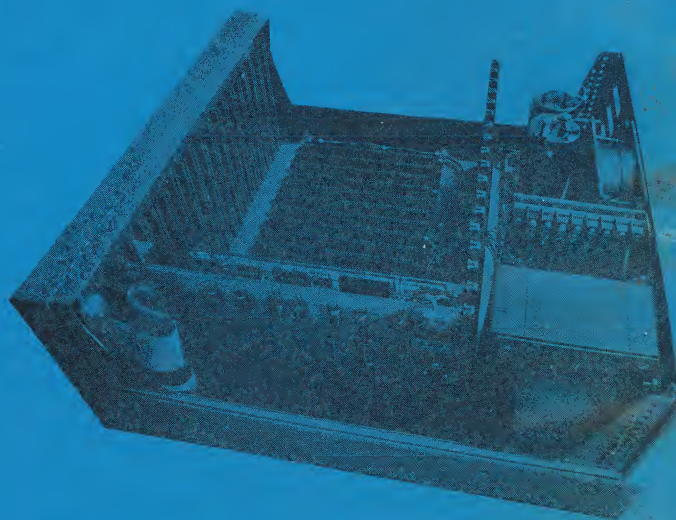
The Memory or I/O operation requires several main signals which allow for transfer of data to and from the CPU. The ADDRESS (A0-A15) signal consists of sixteen individual lines from the CPU to the Memory or I/O device. This signal represents a particular memory address location or external device number which is needed to establish communications with the Memory or I/O Device. Once the ADDRESS (A0-A15) data is presented to the Memory or I/O device, the CPU generates various STATUS signals. The STATUS signals either enable decoding of a memory address, or they condition the I/O device card to send or receive data from the CPU.

Data from the Memory or I/O device is presented on the DATA IN (D10-D17) lines and applied to eight non-inverting bus drivers. The drivers are enabled by a PDBIN signal from the CPU and a BC (bus control) signal. The BC signal is LOW when the Front Panel is not in operation. The eight non-inverting bus drivers, when enabled, present the input data to BI-DATA (D0-D7) lines which apply the data from the Memory or I/O device to the CPU.

Data to the Memory or I/O device is presented on the DATA OUT (D00-D07) lines from the BI-DATA (D0-D7) lines from the CPU. The RDY (ready) line either forces the CPU to a wait state while data is being transferred or allows the CPU to process data.

Front Panel Operation

The Front Panel Operation is very similar to the Memory or I/O operation. The Front Panel gains control of the CPU by producing a HIGH BC signal. The BC signal disables the DATA IN (D10-D17) lines from a Memory or I/O device and enables the FDI0-FD17 lines. The FDI0-FD17 lines contain Front Panel data which is transferred to the CPU upon the occurrence of the PDBIN signal. All data from the CPU to the Front Panel is applied to the DATA OUT (D00-D07) lines and displayed on the Front Panel.



COMPATABILITY

Compatibility

All of the current 8800 software is compatible with the 8800b, and all the current plug-in circuit boards are compatible, with the exception of the 8800a CPU Board.

Memory Cards

1. 4K Dynamic RAM Memory Board
2. 4K Static RAM Memory Board
3. 16K Static RAM Memory Board
4. PROM Memory Board

Interface Cards

1. Serial Interface Board
2. Parallel Interface Board
3. Audio-cassette Interface Board
4. Disc Controller Board

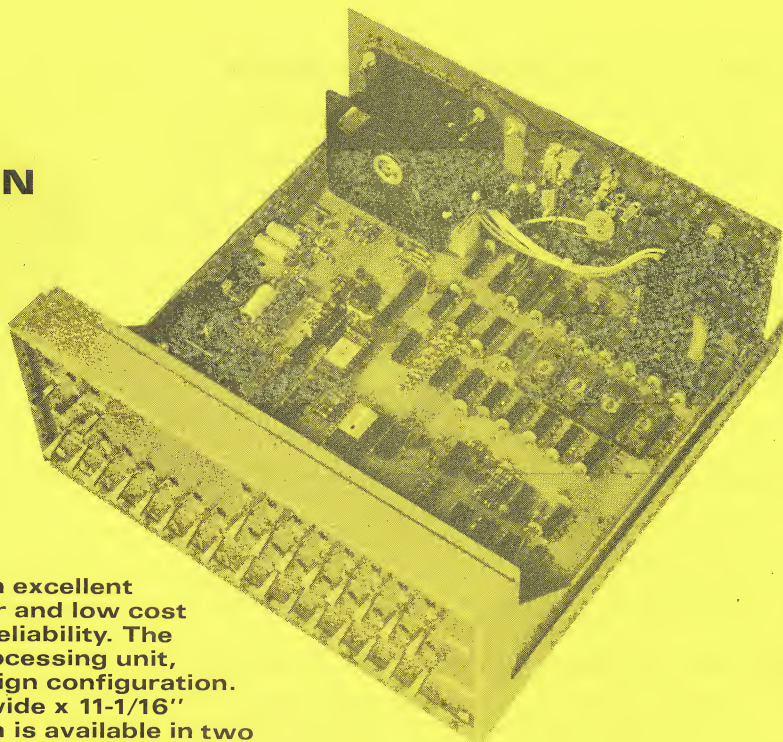
ALTAIR 8800b Specifications	
Number of Boards	Up to 18
Microprocessor	
Model	8080A
Technology	NMOS
Data Word Size, Bits	8
Instruction Word Size, Bits	8
Clock Frequency	2M Hz
Add Time, Register to Register, Microsec. Per Data Word	2
Number of Instructions	78
Input/Output Control	
I/O Word Size, Bits	8
Number of I/O Channels	256
Direct Memory Access	Optional
Interrupt Capability	Std.
Vectored Interrupt (8 priority levels)	Optional
Software	
Resident Assembler	Yes
Higher-level Language	BASIC
Monitor or Executive	Sys. Mon.; text edit.
Complete Software Library Separately Priced	Yes



2450 Alamo S.E. / Albuquerque, New Mexico 87106

altair^{T.M.} 680b

TECHNICAL INFORMATION



The ALTAIR 680b microcomputer is an excellent compromise between computer power and low cost structure, without sacrificing design reliability. The system is based on the 6800 microprocessing unit, which adapts nicely to a minimum design configuration. The ALTAIR 680b measures 11-1/16" wide x 11-1/16" deep x 4-11/16" high. The basic system is available in two configurations, depending on the intended application.

Almost all of the 680b circuitry is contained on a single large printed circuit board, including memory and a built-in I/O port. The full front panel model contains all of the controls necessary to program and operate the computer and includes an additional printed circuit board, which provides all of the logic circuitry necessary to reset, halt or start the processor. Also located on this board are switches and associated LED indicator lights for each of the sixteen address lines and eight data lines. The front panel circuit board mounts directly to the main printed circuit board via a 100-contact edge connector. The power switch is located on the back panel of the unit for safety purposes. A "turn-key" front panel model, which eliminates all control except restarting the processor, is also available.

The basic ALTAIR 680b computer can be subdivided into five functional sections. These are the MPU and clock, the memory, an I/O port, control and indication, and the power supply. The first three of these sections, along with the power supply regulation components, are located on the main printed circuit board.

At the heart of the 680b system is the 6800 Microprocessing Unit, which is largely responsible for the overall simplicity of the 680b design. The 6800 MPU contains three 16-bit registers and three 8-bit registers. The program counter is a two byte register which keeps track of the current address of the program. The stack pointer is also a two byte register which keeps track of the current address of the program and contains the next address in an external, variable length push-down/pop-up stack. The index register is a two byte register used to store data or a memory address for indexed addressing operations. There are two single byte accumulators used for holding operands and results from the arithmetic logic unit (ALU). The 8-bit condition code register indicates the results of an ALU operation. In this register there are two unused bits, kept at a logic one. The remaining six bits are used to indicate the status of the following: carry; half carry; overflow; zero; negative; interrupt.

The 6800 has seven different addressing modes, with the particular mode being a function of both the type of instruction and the actual coding within the instruction. The seven modes include the following: Accumulator Addressing—one byte instructions, specifying either of the two accumulators; Immediate Addressing—two or three byte instructions, with the MPU addressing the location given in the 2nd or 2nd and 3rd bytes when the immediate instruction is fetched; Direct Addressing—two byte instructions which allow the user to directly address the lowest 256 bytes of memory in the machine; Extended Addressing—three byte instructions, the second two bytes referring to an absolute address in memory for the operation; Indexed Addressing—two byte instructions, the second byte being added to the 16-bit index register to give the address of the operand; Implied Addressing—one byte instructions and the instruction itself gives the address; Relative Addressing—two byte instructions where the second byte is added to the lower 8 bits, allowing the user to address memory + 129 to -125 bytes from the location of the present instruction.

There are several timing and control signals required to operate the MPU. Two clock inputs are required, phase 1 and phase 2. These must be nonoverlapping and run at the Vcc voltage level. In the 680b the clock is a 2-MHz crystal controlled oscillator with logic to provide a 500-KHz two phase clock.

Sixteen active high address outputs are used to specify the sections of memory or I/O to be used. These can drive up to one standard TTL load and 130 pf. There are also eight bi-directional data lines with the same drive capability as the address lines.

NEW MEMORY FEATURES

MITS is pleased to announce the development of a 16K static memory card for the Altair 680b. With an access time of 215 nanoseconds and low power consumption of 5 watts, we feel that this is an excellent addition to the Altair 680b.

The 680b cabinet has room for up to three 16K static memory cards, thereby increasing the memory of the Altair 680b to 49K.

SPECIAL FEATURES

PROM monitor.

1702A PROM monitor chip programmed so that you can immediately load and run paper tape object programs such as the text editor and assembler (see below).

Asynchronous Communication Interface Adapter (ACIA).

Allows the machine to transmit and receive a character at a time rather than one bit. Minimizes software needed for I/O routines. Contains crystal clock for baud rate synchronization. User-selectable for RS232, Baudot, TTY, 20ma current loop. Baud rates of 50, 75, 110, 134.5, 150, 200, 300, 600, 1200, 1800, 2400, 4800, and 9600.

Two Pass Resident Assembler and Text Editor

A two pass resident assembler and text editor will be available for assembly language programming. This software is compatible with Motorola's format for assembly language programs, text and object files. 8K bytes of memory are required to run this package. The assembler produces a full assembly listing on the second pass, including the hex codes for the location counter and the instruction mnemonics. A symbol table listing is also produced. The text editor has full capabilities for text editing, including line insertion, printing, deletion and modification; as well as commands for changing one string of characters to another and for searching the text buffers for a particular character string.

Basic Interpreter

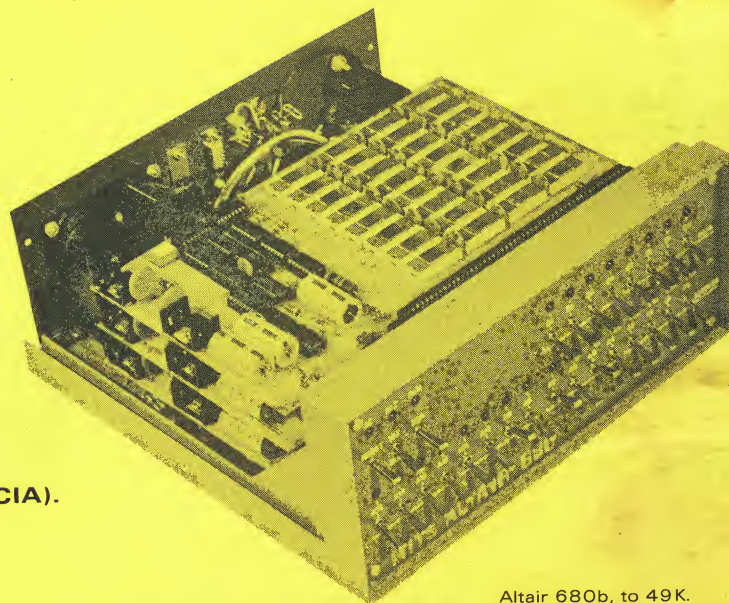
A BASIC interpreter has been developed which will be comparable to the 8800 8K BASIC interpreter.

Buffered Data Lines

All data lines are buffered to provide fanout capability of over 20 standard TTL loads.



The Altair 680b is also available in this Turnkey Model which has a power indicator light and controls for RESET and RUN/HALT on the front panel. The system PROM monitor, when used in conjunction with a terminal, eliminates the necessity for toggling front panel switches to load bootstraps or to examine and change memory contents.



Altair 680b, to 49K.

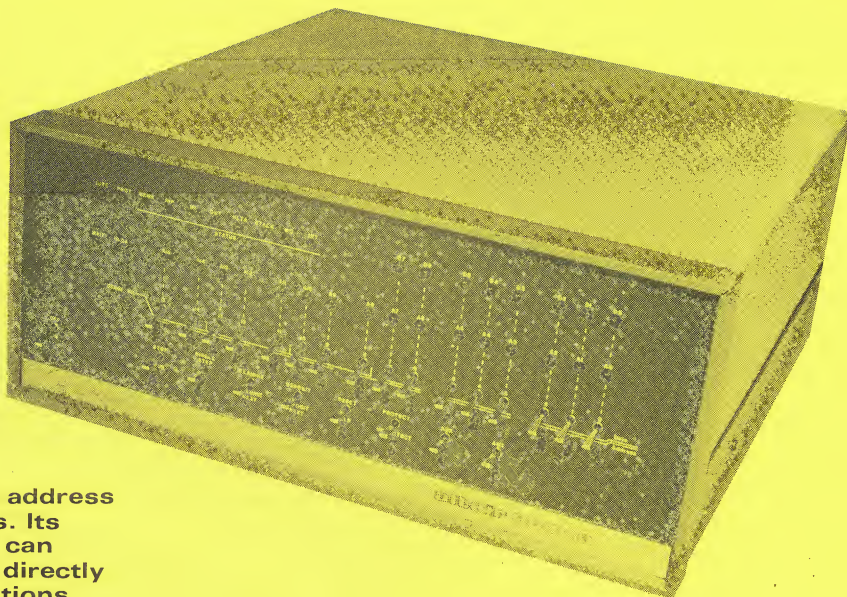
Altair 680b Specifications	
No. of Boards	Up to 3 additional
Microprocessor	
Model	6800
Technology	NMOS
Data Word Size, Bits	8
Instruction Word Size, Bits	8
Clock Frequency,	500KHz
Add Time, Register to Register,	
Microsec. Per Data Word	2
Number of Instructions	72
Input/Output Control	
I/O Word Size, Bits	8
Number of I/O channels	256 Memory Address Locations Designated
Interrupt Capability	Std.
Type of Interrupt System	Maskable (Interrupt Request) and Non-maskable Interrupt
Software	
Resident Assembler and Editor	Yes
Higher-level language	BASIC
Monitor	Resident System Monitor on PROM
Complete Software Library	
Separately Priced	Yes



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altair 8800a^{T.M.}

TECHNICAL INFORMATION



The Altair 8800a is a parallel 8-bit word/16-bit address computer with an instruction cycle time of 2 μ s. Its central processing unit is the 8080 LSI chip. It can accommodate 256 inputs and 256 outputs, all directly addressable, and has 78 basic machine instructions. It is capable of directly addressing up to 65,000 bytes of memory.

As well as the LSI chip, the CPU board contains the two-phase clock, status latch, buffers and the various lines going to the bus. (The buffers are tri-state devices.)

The CPU contains six general-purpose registers, P counter, arithmetic unit, accumulator, stack pointer, instruction decoder, and miscellaneous timing and control circuits. The arithmetic unit contains the circuitry required to perform arithmetic in both decimal and binary forms. The stack pointer defines the current address of the external stack, which resides in memory. The stack is used to service interrupts and provides virtually unlimited subroutine nesting. The instruction decoder decodes the instructions and sets up the various registers, gates, etc., in the CPU for proper functioning.

There are 36 LED status indicators on the front panel, 16 of which are used for the address bus, 8 for the system status latches, and 8 for the data bus. The four remaining LEDs are used for indicating memory-protect, interrupt-enable, system-wait and hold status. Address line inputs A0 through A15, data lines D0 through D7, and the various status lines originate on the CPU board.

The front panel control board contains the circuitry for interfacing between the control switches located on the front panel and the CPU. In addition to the interconnections to the actual processor, this board accepts memory address switches A0 through A15 (also on the front panel). The first eight of these switches (D0 to D7) are used to put data into the CPU.

The front panel logic permits the following functions: STOP—stops the processor immediately after it completes the current instruction; RUN—starts the processor at the current address; EXAMINE—causes the data stored at the location (set by the switches) to be displayed in binary by LEDs; EXAMINE NEXT—steps the P counter once and displays the word

stored at the next location; DEPOSIT—causes the information preset by the switches (A0-A7) to be stored in memory; DEPOSIT NEXT—steps the P counter and loads the memory; SINGLE STEP—steps the program one machine cycle; RESET—clears the CPU and sets up a starting address of 0; PROTECT/UNPROTECT—allows selective write protection of blocks of memory. When a block of memory is protected, it is impossible to write over that block, but its contents can be read out.

With proper adjustments, any memory speed can be used in the 8800a computer, although memory access time must be 500 nanoseconds or less if it is to be run without wait states. In addition to semiconductor RAMs, the processor will also service ROMs and PROMs.

NEW FEATURES

POWER SUPPLY

The power supply provides three voltages to the 8800a bus: +8V pre-regulated at 8 amps; +15V at 500mA; -15V at 500mA.

FAN

A fan has been mounted on the back panel of the 8800a to provide cooler operating temperatures.

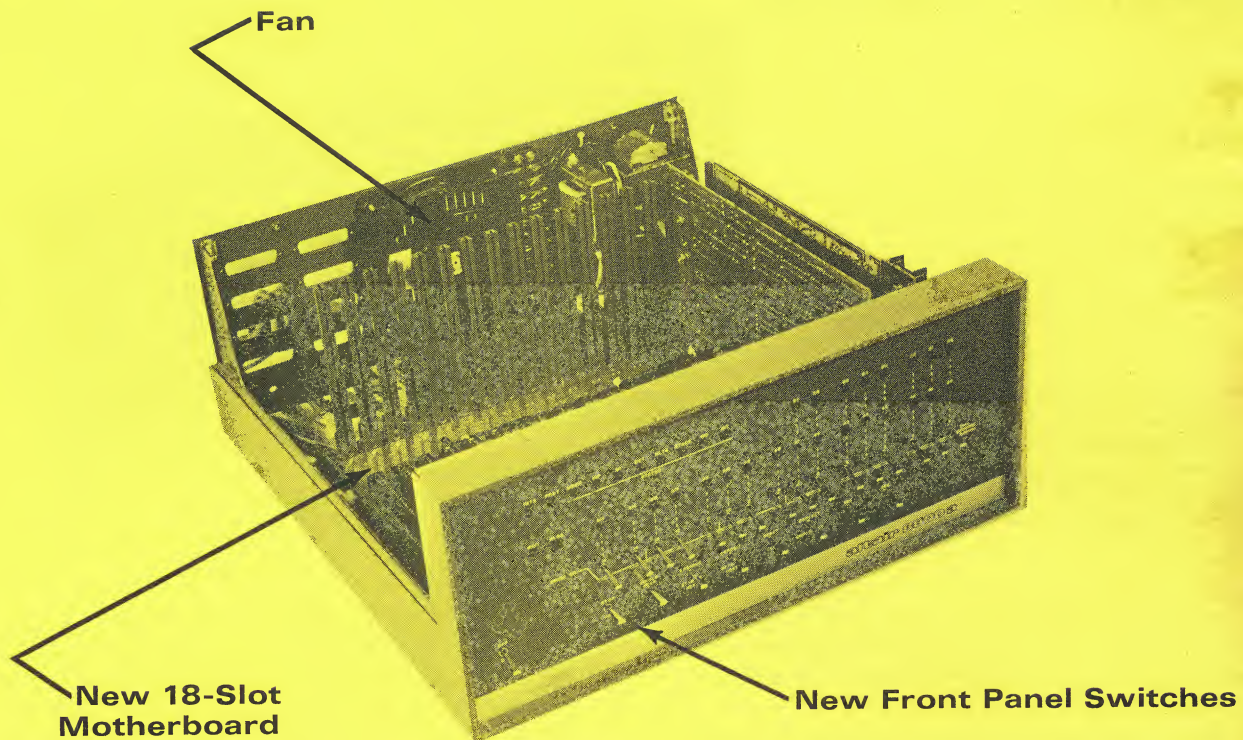
18 SLOT MOTHERBOARD

The four-slot expander cards in the Altair 8800 have been replaced with a single-piece 18-slot motherboard. The 18-slot motherboard contains the 100 solder lands that comprise the 100 pin bus.

FRONT PANEL SWITCHES

The front panel toggle switches have 50% longer handles that are flat (instead of round) for easier use.

An assembled Altair 8800a may be ordered with six, twelve, or eighteen sets of edge connectors. The Altair 8800a kits include an edge connector with every plug-in module purchased.



The four boards, along with the power supply, mount in an 18" deep x 17" wide x 7" high (45.7 x 43.2 x 17.7-cm) metal cabinet.

SPECIFICATIONS

Number of Boards	Up to 18
Microprocessor	
Model	8080A
Technology	NMOS
Data Word Size, Bits	8
Instruction Word Size, Bits	8
Clock Frequency,	2MHz
Add Time, Register to	
Register, Microsec.	
Per Data Word	2
Number of Instructions	78
Input/Output Control	
I/O Word Size, Bits	8
Number of I/O Channels	256
Direct Memory Access	Optional
Interrupt Capability	Std. one level
Vectored Interrupt (8 priority levels)	Optional
Software	
Resident Assembler	Yes
Cross Assembler	No
Simulator	No
Higher-level Language	BASIC
Monitor or Executive	Sys. mon.; text edit.
Software Separately Priced	Yes



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Technical Information

altairTM Floppy Disk (88-DCDD)

The 88-DCDD consists of the Disk Controller and one Disk Drive with an interconnect cable. The Disk Controller consists of 2 PC boards (over 60 ICs) that fit in the Altair chassis. The Disk Drive unit consists of a PERTEC FD-400, a power supply PC board, and a Buffer/Address/Line Driver PC board. The Disk Controller converts the serial data to and from 8-bit parallel words (one word every 32 microseconds). The Disk Controller also controls all mechanical functions of the disk as well as presenting disk status to the computer.

Software and System Features

Altair Disk Extended BASIC is an enhanced version of Altair Extended BASIC with added capabilities for saving and loading programs, and for manipulating data files on disk.

Altair Disk Extended Basic uses random and sequential files for storing information on disk.

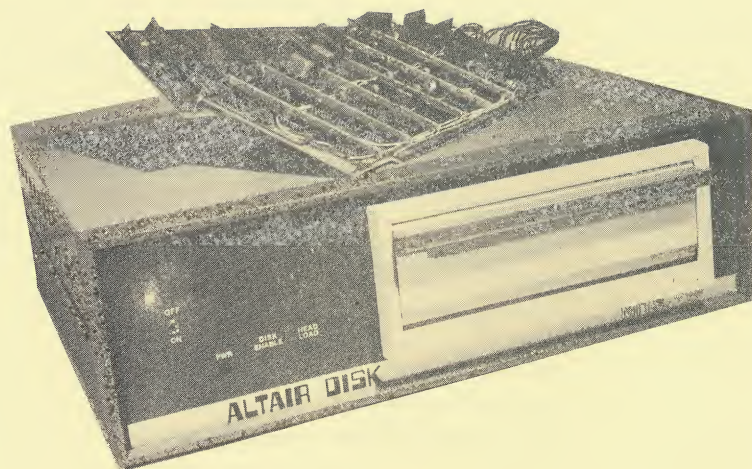
Utility software is included with Altair Disk Extended BASIC for copying diskettes, initializing blank diskettes, listing directories, etc.

Disk bootstrap loader is available on paper tape, cassette tape, or PROM (used with 88-PMC PROM Memory Card).

Hard sector format (non IBM compatible) allows storage of over 300,000 data bytes.

Altair Disk Extended BASIC requires a minimum of 20K of RAM memory to operate in.

PROM Disk Bootstrap loader allows loading of Altair Disk Extended BASIC in less than 10 seconds from the time power is turned on.



Hardware

A. Description and Features

The Disk Controller, which acts as the interface between the Altair and the Disk Drives, consists of 2 PC boards that fit in the Altair chassis. They require 2 slots in the Altair, contain over 60 ICs, and connect to the Disk Drives via an 18 pair flat cable. The Controller can address up to 16 drives.

The Disk Drive Unit consists of a Pertec FD-400 drive in an Optima case 5½" high, 17" wide, and 17½" deep (same width and depth as the Altair 8800). Also in the Disk unit is a power supply and a Buffer/Address card for selecting the drive and interconnecting multiple disk systems. A fan is included to maintain low ambient temperature for continuous operation. The Disk Drive units interconnect to each other in daisy chain fashion and to the controller using 18 pair flat cables and DC-37 type 37-pin rectangular connectors.

B. Hardware Specifications

Access Time:

Track to track: 10 ms.

Head load and settle time: 45 ms.

Average time to read or write:
400 ms.

Worst case: 1135 ms.

Rotational speed: 360 RPM (166.7
ms/rev)

Tracks: 77 per disk

Sectoring: Hard sectored, 32 sectors
per track, 5.2 ms/sector (non IBM
compatible)

Data Transfer Rate: 250,000 bits/sec.
(one 8-bit byte every 32 microseconds)

Maximum number of drives per system: 16

Data storage capacity: 310,000
bytes per disk

Data bytes per sector: 128

Data bytes per track: 4,096

Disk Drive head life: over 10,000
hours of diskette to head contact

Disk Drive MTBF: exceeds 4,000
hours

Disk Drive data reliability: not more
than 1 in 10^9 soft (recoverable errors,
1 in 10^{12} hard (non-recoverable errors

Power:

Controller: 1.1 amps at + 8V unregu-
lated (from Altair bus)

Disk Drive Unit: 110 watts 50/60
Hz 117/220 VAC

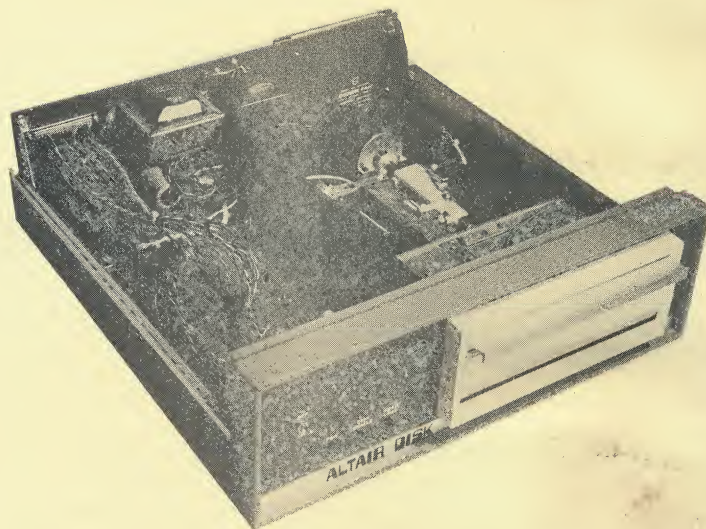
Diskette: Hard sectored, 32 sectors +
index hole (Dysan #101, ITC #FD
32-100)

Disk Drive Unit Weight: 40 pounds

C. Operating Principle

The Disk Controller cards provide the interface between the Disk Drive Unit and the Altair bus. Serial read data from the disk is converted into 8-bit parallel form by the controller for transfer to memory via the CPU. Data is written on the disk by converting the 8-bit bytes outputted from the Altair CPU to serial form. All read and write data is transferred one byte at a time through the CPU.

Disk Controller Board #1 controls I/O address selection, sector counting, read data, and disk status. Disk Controller Board #2 controls disk drive addressing, write data, and disk drive functions.



Ordering information:

1. 88-DCDD

Includes:

- Set of controller cards
- 1 Disk Drive Unit
- 1 interconnect cable—6 ft. long
- 1 Assembly and Operators Manual
- 1 Disk Extended BASIC Manual
- 1 Blank Diskette

2. 88-DISC

Includes:

- 1 Disk Drive Unit (117 VAC unless otherwise requested)
- 1 Interconnect cable—6 ft. long
- 1 Blank Diskette

3. Altair Disk Extended BASIC

Requires a minimum 20K of memory for operation.

Includes:

- Altair Disk Extended BASIC on diskette
- Altair Disk Extended BASIC Manual
- Paper tape or cassette magnetic tape bootstrap loader (specify when ordering)

4. Disk Bootstrap Loader on PROM:

Order 88-PMC (PROM Memory Card) and DBL PROM (PROM programmed with disk bootstrap loader routine)

5. Manuals only:

- Disk Hardware Manual
- Altair Disk Extended BASIC Manual



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Vector Interrupt / Real Time Clock (88-VI/RTC)

The 88-VI gives the computer the capability to interrupt activity via the Restart (RST) instruction and to allow only the highest active priority of the 8 priority levels to interrupt the CPU.

The Real Time Clock provides the computer user with the capability to interrupt the processor at one of four selectable rates. The RTC generates an interrupt after a precise interval of time, which enables software to time certain routines and even to generate the correct time, day, and year, upon request.

The RTC source may be selected from either a derivative of the 2 megahertz clock or the line frequency. The 2 megahertz clock should be used if a fast RTC is needed; it is selectable for time intervals down to every 100 microseconds. The line frequency (60 Hertz) should be used in systems that require accuracy over a long period of time.

Hardware

Altair Slots: One.

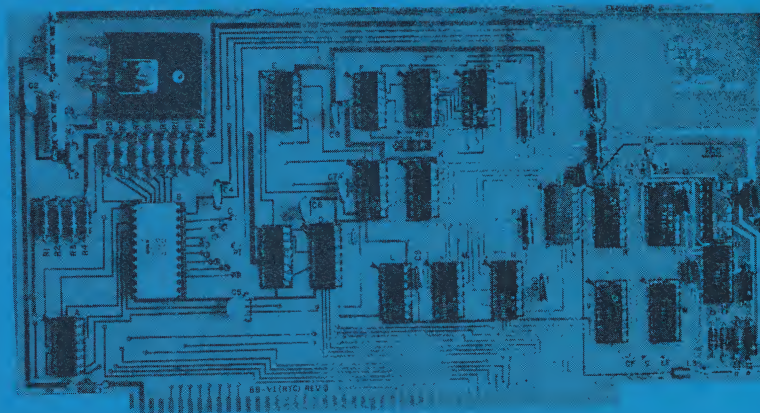
Power: 5 volts at 300 ma.

Operation

ENABLE INTERRUPT instruction of the computer permits interruption. ENABLE INTERRUPT must also be activated after each interrupt is completed in order to reactivate the CPU's internal interrupt.

RST is an instruction which translates in octal code to 3N7; where "N" is a 3 bit code which represents one of the 8 priority locations, 0, 10, 20, 30, 40, 50, 60, or 70 (octal). Restart instructions are RST0=307, RST10=317, RST20=327, etc. (octal). The vector interrupt places the RST instruction on the data bus at the correct time.

The 88-VI directs the interrupt to one of its 8 bus lines (VI0-VI7). VI0 is the highest priority, VI7 is the lowest.



The RST address will direct the computer to the highest active VI bus line. When an interrupt occurs that is higher priority than the active interrupt, the 88-VI interrupts the CPU and puts the RST instruction and the 3-bit address associated with that priority level on the data bus.

The Interrupt Service Handler is the software device which supervises all individual device service routines. Interrupt Service Handler enables the interruption of a lower interrupt routine by a higher one and also insures that each lower routine will be returned to and fully executed.

Address: Address 376 (octal). Bits 0, 1, 2, and 3 are used to update current level status. Bit 6 is used to enable/disable the Vector Interrupt feature.

The Real Time Clock offers 2 clock sources: the system clock (operates at 2 megahertz), or the line frequency (operates at 60 hertz). The system clock interrupts once every 100 microseconds, 1 millisecond, 10 milliseconds, or 100 milliseconds. Line frequency interrupts once every 16.67 milliseconds, 166.7 milliseconds, 1.667 seconds, or 16.07 seconds. Any of the selected time intervals may be used to interrupt at any one of the 8 priority levels.

Clock Source Intervals:

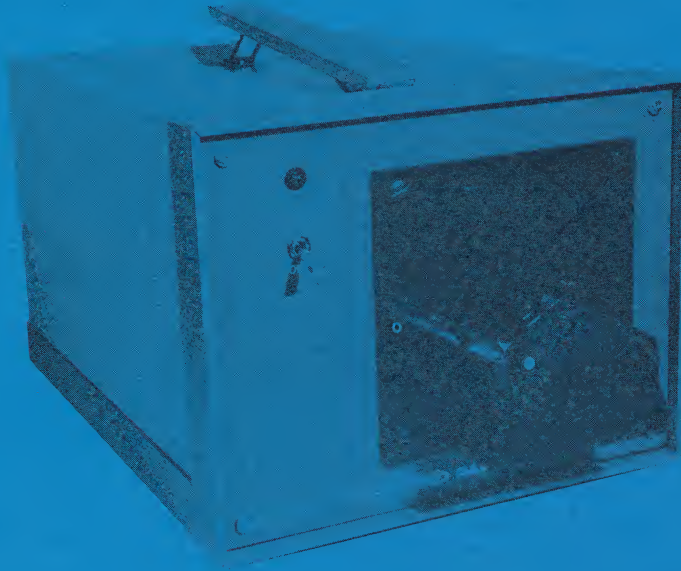
System Clock [2MHz]: 100 ns, 1 ms, 10 ms, or 100 ms.

Line Frequency [60Hz] Intervals: 16.67 ms, 166.7 ms, 1.667 sec., or 16.67 sec.

Accuracy: 2MHz, .01%.



High Speed Paper Tape Reader (88-HSR)



Specifications

Reading Speed: 30 cps or 300 cps, software selectable, stops "on character"

Tapes:

Light transmissivity: 57% or less

Thickness: .0027-.0045 inch

Type: standard 8-track (1-inch) and most other standard 5, 6, or 7 track

Data Output: TTL:

a. Less than .4 volts at 16 ma (no hole);
2.4-5 volts at .2 ma (hole).

b. Plus-in compatible with 88-4PIO or Altair 680 parallel port.

The High Speed Paper Tape Reader design is based upon the REMEX 300-character-per-second opto-reader. The 88-HSR connects directly to 1 port of an 88-4PIO parallel interface card or 1 parallel port of an Altair 680b computer.

Hardware

Dimensions: 6½" high x 8½" wide x 11" deep.

Drive: DC stepping motor with sprocket drive.

Power: 50 watts, running.

READ Mechanism: Filament lamp to fiber optics to photo cells. The lamp is operated below voltage rating to greatly prolong life.

Tape loading: Easy in-line front load.

Software Features

Start/stop on character.

Low power standby mode. The standby mode reduces motor voltage during periods of inactivity, and allows tapes to be read at the reduced speed of 30 cps.



2450 Alamo S.E. / Albuquerque, New Mexico 87106

Technical Information

AUDIO CASSETTE RECORD INTERFACE (88-ACR)

The 88-ACR allows reading and writing of data on audio cassettes, using frequency modulation. The 88-ACR may be used with any medium (or better) quality cassette tape. (Music quality recorders generally give better performance than smaller portable recorders.)

Features

The 88-ACR may be used with machine language Read/Write programs or with ALTAIR BASIC commands (8K and Extended versions).

ALTAIR BASIC commands, CSAVE and CLOAD, are used to save and load programs or data arrays through the 88-ACR.

ALTAIR software is available on audio cassette tapes for loading into the ALTAIR through the 88-ACR.

Uses any tape recorder with less than 2% wow and flutter. The better the speed stability, the better the data integrity.

Hardware

General Description:

Consists of 88-SIOB (Serial I/O Board) mated to a MODEM (Modulator/Demodulator) board.

Requires one slot in the ALTAIR bus.

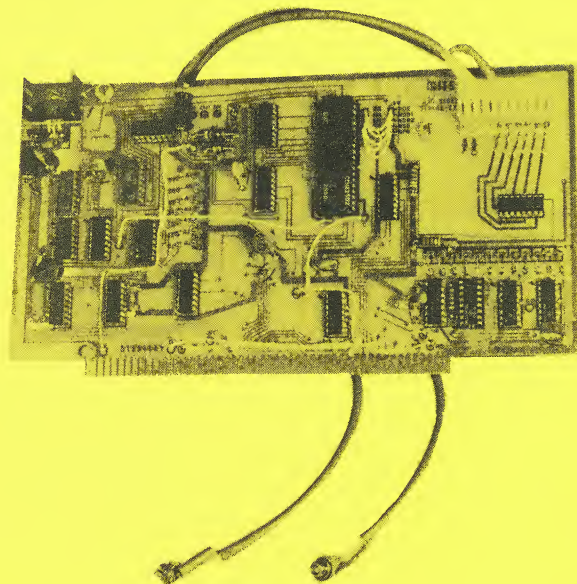
Connects to a tape recorder via miniature phone jacks (user supplies the interconnect cord).

MODEM Circuit Operation

Operates by frequency modulating audio frequencies in the record (write) mode, and demodulating these tones in the play (read) mode.

To record data, digital information from the ALTAIR is changed to audio frequencies by dividing the 2MHz system clock at different rates. A logic 1 gives a 2400 Hz tone, a logic 0 gives an 1850 Hz tone.

To read data, audio tones are filtered and then demodulated by a phase locked loop.



88-SIOB Operation

Digital information is in Universal Asynchronous Receiver/Transmitter (UART) format (start bit, 8 data bits, stop bit) at 300 baud.

The UART converts ALTAIR write data from parallel to serial form for the modulator.

The UART converts serial read data from the demodulator to parallel form for the ALTAIR.

Specifications

Modulation Frequencies: Logic 1-2400 Hz, Logic 0-1850 Hz.

Data Rate: 300 baud, 30 bytes/second.

Bit Format: UART type (1 start bit, 8 data bits, 1 stop bit).

Output Level: 100 MV p-p sawtooth, suitable for "MIC" input of recorders.

Output Impedance: 1.5K ohms.

Input Level: 200 MV p-p to 10 V p-p.

Input Impedance: 100K ohms.

Speed Tolerance: 2% without adjustment of PLL, 5% with adjustment of PLL.

Connector Type: 3.5 mm (1/8 in.) miniature phone jack.

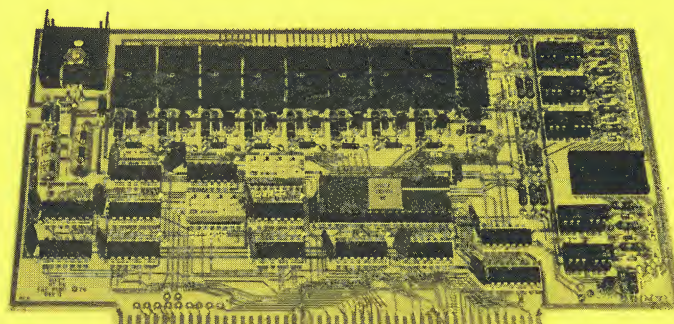


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Technical Information

Altair™ 88-Process Control Interface (88-PCI)

Introduce your Altair 8800b to the diverse world of electrical, mechanical and sensory devices with the addition of the 88-Process Control Interface. By relaying various types of sensory information to the computer, the 88-PCI permits a wide range of control applications.



Applications

Whether your applications revolve around industrial, scientific, business, communication or household uses, the potential of the 88-PCI is virtually unlimited.

Some possible industrial applications include a product sorting and grading system. The 88-PCI can be interfaced with various kinds of sensors for measuring size, weight, optical density and other properties while controlling a sorting mechanism.

In the field of scientific research, an 88-PCI may be used to control environmental test conditions. Test responses can be gathered either by an 88-AD/DA converter or by the 88-PCI.

Suggested household uses include: control of thermostat settings, manual switches, lighting, lawn sprinkling and other home operations.

Features

The board consists of an eight relay output section, with each relay capable of switching 120v AC at 1 amp. Eight opto-isolators which can be configured by the user to accept a wide range of voltages make up the input section. Four more opto-isolated signal lines are arranged as two pairs of handshake lines, with the input section and output section each having one handshake pair. These lines are for control of and communication with external devices. All of the lines are completely isolated and balanced for use in environments with high levels of electrical noise.

Operation

When the board is set-up and initialized, relay control is accomplished by outputting an eight bit word to the relay control channel. Logic "1" lines will energize their respective relays, and those set to "0" will de-energize. An input from the opto-isolator input channel reads the data from the opto-isolated input lines. The interrupt structure and use of the handshake lines are under software control.



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88-Analog to Digital/ Digital to Analog Converter (88-AD/DA)

Another new option has been added to the growing line of Altair 8800 series peripherals. The 88-AD/DA is an eight channel analog I/O subsystem, allowing the acquisition and digitizing of analog data ranging from 0 to 10 VDC. Digital to analog conversion produces a 0 - 10 VDC output available in 256 steps of 39 millivolts. With the 88-AD/DA, the Altair 8800 microcomputer can measure analog voltages and generate them to eight bit accuracy.

Applications

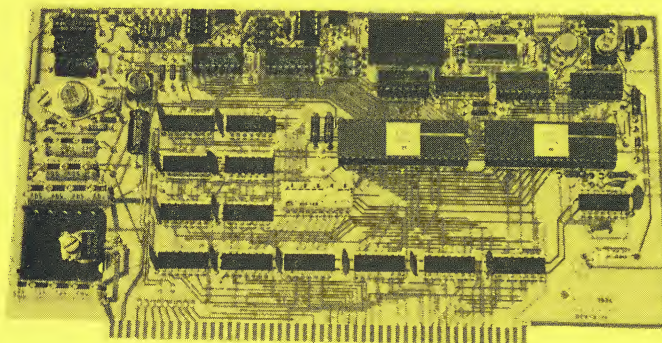
The versatility of the 88-AD/DA allows user implementation for many applications where analog to digital and digital to analog conversion is necessary. 88-AD/DA operation may be implemented for computer control, graphics production, games, scientific/electronic experimentation and monitoring.

Some suggested inputs and sources from which data can be obtained include joysticks (games, remote control, graphics), transducers (light, pressure, temperature), magnetic tape and instrumentation amplifiers (biomedical, chemical, circuit and acoustical analysis).

Oscilloscopes, magnetic recorders, meters and music synthesizers (voltage controlled oscillator, voltage controlled filter) are just some of the output devices to which data transfer is possible.

Operation

The 88-AD/DA Converter is an analog subsystem that functions as an Input/Output (I/O) device. Analog data is input to an eight channel Multiplexer and converted to a digital equivalent value by a successive approximation type Analog-to-Digital Converter. Sample and Hold is provided to insure accurate conversions even for rapidly changing signals, and on-board timing is available to control sequencing of the Sample and Hold and Successive Approximation Register. From the time the Multiplexer has a valid address, 10 to 12 μ s must elapse before the conversion data is available to the system. The conversion time for the Analog-to-Digital Converter itself, without settling time allowed for the Sample and Hold, is less than 5 μ s.



The 88-AD/DA Converter board contains two Digital-to-Analog Converters that may be used to provide low cost analog output. The conversion time for each converter is limited only by the slew rate. The slew rate of the Digital-to-Analog Converters is adjustable with an on-board feedback capacitor to a maximum rate of approximately 50v per μ s. The 88-AD/DA Converter board features 8 bit resolution for both A to D or D to A sections.

Specifications

AD Section

Input Mux Channels: 8
Resolution: 8 bits
Monotonicity: 8 bits
Sample and Hold Settle Time: 5 μ sec.
Conversion Time: 5 μ sec:
Time from Start Conversion
to conversion complete: 11 μ sec.
Nominal Input Range: 0-10 VDC
(39mV per step)

DA Section

DA Converters: 2
Resolution: 8 bits
Monotonicity: 8 bits
Settle Time: 85ns (50v/ μ sec)
Nominal Output Range: 0-10 VDC
(39 mV per step)

Power Requirements

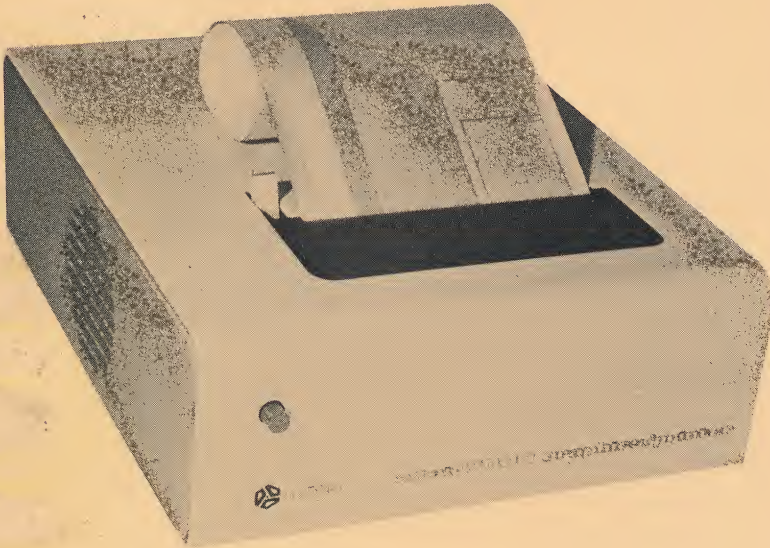
+ 18V unregulated at 45mA
- 18V unregulated at 47mA
+ 8V unregulated at 450mA



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7000 Graphics/Printer

TECHNICAL INFORMATION



The 7000 Graphics/Printer is a multi-function, hard-copy output system which acts as a printer, plotter and graphics device. Its tremendous flexibility makes it one of the fastest and most economical methods of electrostatic printing available. The 7000 uses eight software-driven print electrodes instead of the usual seven found in 5 x 7 matrix printers.

Features

Printed output can be made for about 1 cent per foot of electrosensitive paper. The 7000 is plug compatible with the 8800 mainframe via one PIO port. For graphics: An extra printing electrode provides symmetry along the horizontal and vertical axes to permit plotting. Either a distinct outline or a sophisticated detailed picture with shaded areas can be produced.

Extended or Disk Extended BASIC with the 7000 option must be used with the 7000 Graphics/Printer. The software for plotting (written entirely in BASIC) allows the user to make custom modifications and save room in memory by removing unnecessary subroutines. Listings of the plotting subroutines are supplied free of charge with the printer.

The BASIC subroutines consist of:

1. performing initialization (setting buffer size, location, etc.)
2. printing the entire buffer
3. clearing the buffer
4. marking a dot
5. writing a character
6. writing a string for a label
7. calculating scaling factors
8. plotting a point
9. drawing a line

Power: 115 VAC, 36 VA

Weight: 14 lbs.

Input Raster: 8-bit parallel

Capabilities

Line widths of 20, 40 or 80 characters within a 4-inch margin (upper and lower case)

Printing Speed: 160 characters per second (80 characters per line) or 120 lines per minute.

Horizontal Resolution:

1. Internal Timing: 80 dots/inch
2. External Timing: better than 128 dots/inch

Vertical Resolution: 65 dots/inch

Printhead Speed: 0.0175 inches/msec.
 $\pm 0.1\%$

Timing Markers:

1. Every 1/80 inch of printhead travel (Dot Timing)
2. Every 1/10 inch of printhead travel (Character Timing)

Plotting Speed: 2 lines per second, 8 dots vertical per line

Operation

The 7000 is controlled by using a single port on an 88-4PIO parallel interface board. One section of the port provides the 8 bits of information to be printed; the other section provides control. Each time a new column of information is to be printed, the appropriate data bits are forced low by the 4PIO. Each low data line causes the related printhead electrode to discharge to the paper, which produces a dot. There is a total of more than 500 8-dot columns in a line.

In the graphics mode, the image to be printed is stored in memory with a buffer. Each bit represents one dot in the picture. A 256-byte memory segment represents the 8 rows of 256 dots printed on one pass of the printhead. Since an 8 x 256 dot picture is far too small for practical purposes, the plot routine uses a number of these 8 x 256 elements to compose a picture. The standard number is 32 which requires an 8K buffer. The number of elements used may be increased or decreased by altering a single BASIC statement.



Technical Information

4-Port Parallel I/O Board (88-4PIO)

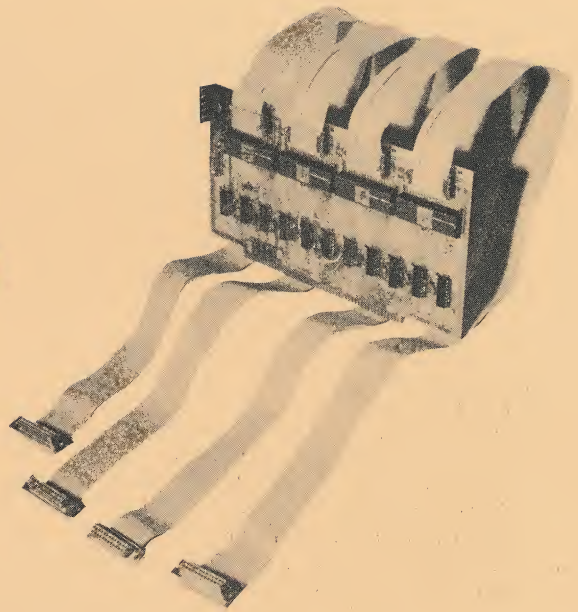
The 88-4PIO board design is based upon a peripheral interface integrated circuit. The chip contains all control and data registers, thus most 88-4PIO options are software selectable. These options include data direction (each data line can act as input or output) and interrupt/control structure modification. The 88-4PIO board can be expanded to four "PORTS" (four 6820 ICs), making it one of the most powerful and versatile interface boards available.

Hardware

The 4PIO board connects to the back panel of the computer with a removable flat cable. The cable has a 24-pin removable plug on the board, and a 25-pin connector on the back panel.

Altair slots: One.

Power: + 5 volts at 500 milliamps with 4 ports.



Capabilities

The 4PIO board is capable of handling up to 4 ports on one plug-in card. Each port contains 16 data lines. Each line can be initialized as input or output to interface a terminal (8 lines in, 8 lines out).

The 4PIO board can handle 2 inputs (such as a paper tape reader and keyboard) or two output devices (such as a paper tape punch and printer) or any combination of custom applications.

All data lines are fully TTL compatible.

Eight of the 16 lines are capable of directly driving the base of a transistor switch (1.5V at 1 ma).

A 4PIO with 4 ports has 64 data lines (each group of 8 is individually selectable) and consumes 500 ma at 5V—typical.

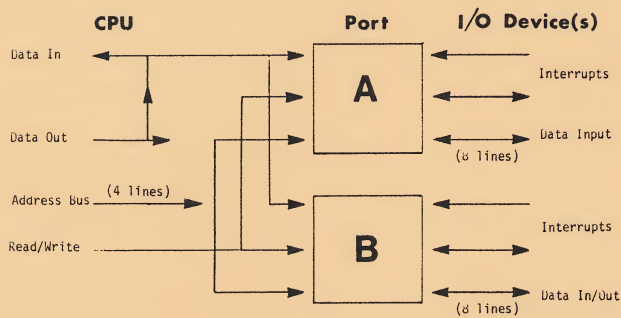
Interface—Parallel; 16 data lines, 4 control/interrupt lines; TTL compatible input and output, plus 8 of the 16 data lines can drive 1.5 volts at 1 milliamp for transistor compatibility.

Bit Configuration : Each data line can be software selected to act as an input or output.

Operation

Each port provides 4 controllable handshake lines. These lines are enabled/disabled under software control. Two interrupt lines are capable of acting as outputs for ready/busy handshake. There are 2 control/status registers which contain a status bit for each of the 2 interrupt lines to the CPU.

The following simplified block diagram demonstrates the address-register operation of one port on the 88-4PIO:



Assuming that the board is addressed at location 0, register selection for port 0 is:

Address	Register
0	Section A—Control
1	Section A—Data
2	Section B—Control
3	Section B—Data

Port 1 includes addresses 4, 5, 6, and 7;
Port 2 includes addresses 8, 9, 10, and 11;
Port 3 includes addresses 12, 13, 14, and 15.

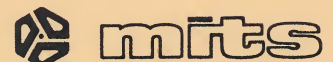
Control/Status—Each 8-bit section:

- Input : sets flag and/or interrupt line
- Input: acts as above
- Output: acts as "busy" signal back to the device.

Interrupt Structure—Each 8-bit section:

- Interrupt request signal to CPU or 88-VI.
- 2 interrupt status bits, 1 for each of above control lines.

Address Select—Each port requires 4 addresses.



16K Static Memory Board (88-16MCS)

The 88-16MCS design is based upon a 4,096 x 1 bit static random access integrated circuit. These RAMs offer the advantage of low power consumption and extremely fast access time, and also eliminate the need for additional refresh logic common to dynamic memories.

Hardware

Dimensions: 10" x 5"

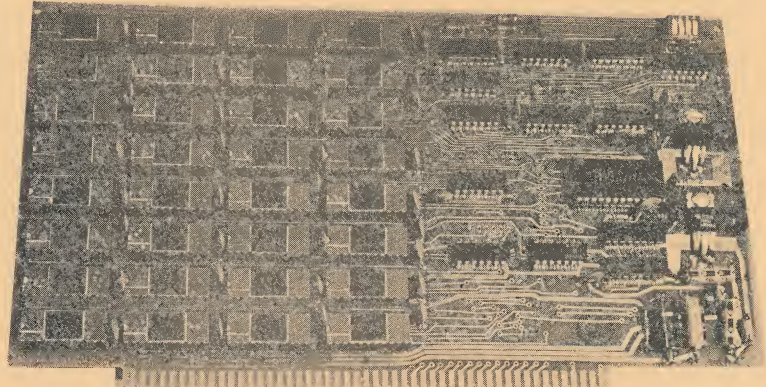
Altair Slots: One

Power: +5V (400 mA, Max.), +12V (200 mA, max.), -5V (100 mA).

Epoxy solder masks cover areas not to be soldered.

Sockets are provided for all RAM ICs.

A DIP Switch is used for board address selection.



Capabilities

Provides 16,384 8-bit words of Random Access Memory on one card.

Access Time: 215 ns.

Cycle Time: 390 ns.

Operation

There are no wait states (due to fast access time).

Since only four 88-16MCS boards are required for the maximum amount of memory directly addressable by the computer, only the upper two address bits are required to select a particular board. The upper four address bits select a single 4K block on a particular 16K card. The remaining twelve address bits are buffered and inverted to select one location within a block.



Technical Information

Synchronous 4K Memory Board (88-S4K)

The 88-S4K Board is totally synchronous — this means that the board relies solely on the CPU for timing signals (no single shots). The S4K provides 4,096 bytes of Random Access Memory. Each board contains memory protect circuitry, and address selection circuitry for any one of 16 starting address locations in increments of 4K.

Hardware

Dimensions: 10" x 5"

Altair Slots: One

Power (worst case):

+ 5V at 450 milliamps

+ 12V at 290 milliamps

+ 12V at 10 milliamps (unselected)

Operation

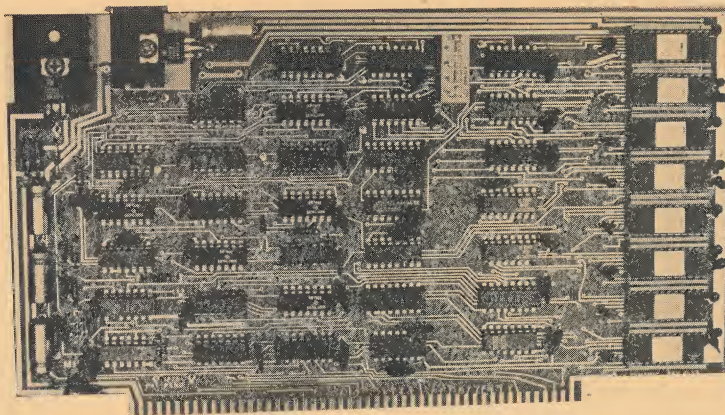
Runs at maximum speed (no wait states).

No hardwire jumpers.

A DIP switch is used for board select.

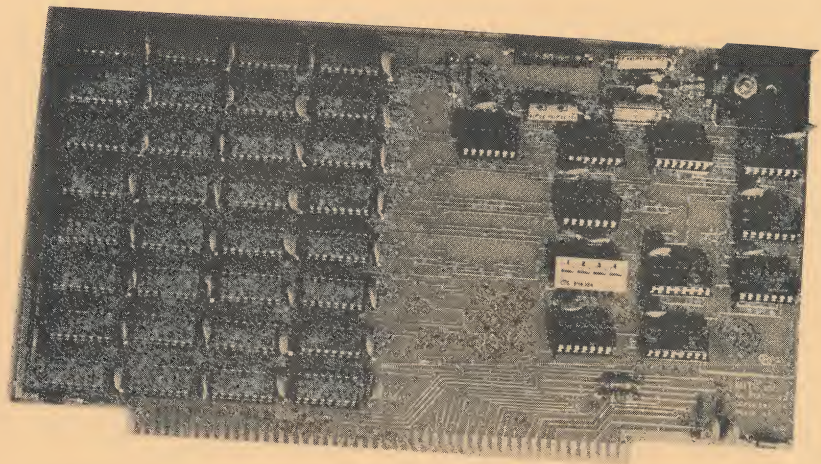
The entire 4,096 bytes of memory can be protected by switching to PROTECT.

Access Time: 200-300 ns.



Technical Information

4K Static RAM Board (88-4MCS)



Technical Information

The 88-4MCS consists of four 1024 by 8 bit memory arrays, an Address Select Circuit, a Read Circuit, a Write Circuit, a Memory Protect Circuit, and a voltage regulator. The board operates by retaining data in its memory cells, each cell having a unique location, or address.

Hardware

A solder mask on the soldered side of the PC board helps prevent solder bridges during assembly.

A DIP Switch for address selection (no address jumpers).

Sockets for all logic and memory ICs.

Power: +8V unregulated at 1.2A, Max.

Access Time: 450 ns., worst case;
300 ns., typically.

Operation

To place information (in 8-bit binary form) in a memory cell, the CPU (Intel 8080 in the Altair 8800) performs a write function, usually caused by a Store Data instruction or a Move Data to Memory instruction. Data may also be stored in memory by using the Deposit Switch on the Altair Front Panel.

To read data from memory, the CPU must perform a Read Data operation. This is a normal function since the CPU must "fetch" data stored in memory in order to perform the necessary operations. The data in memory may be instructions for the CPU or data for the CPU to manipulate.

Data is stored in the Altair 8800 memory in groups of 8 bits, called words or bytes. The Altair can directly address up to 65,536 bytes of memory (sixteen 4K boards).



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Technical Information

PROM Memory Card (88-PMC)

The 88-PMC is a Programmable Read Only Memory (PROM) card designed for programs that must be retained if power to the computer is interrupted. It is capable of providing up to 2K bytes of PROM memory using either the 1702 or 1702A type PROMs (8 bits by 256 bytes per PROM).

Hardware

Dimensions: 10" x 5"

Altair Slots: One

Power: + 8V at 500 ma - 16V at (*) ma

*30-50 mA/PROM with PROM "on"

5-10 mA/PROM with PROM "off"

Capabilities

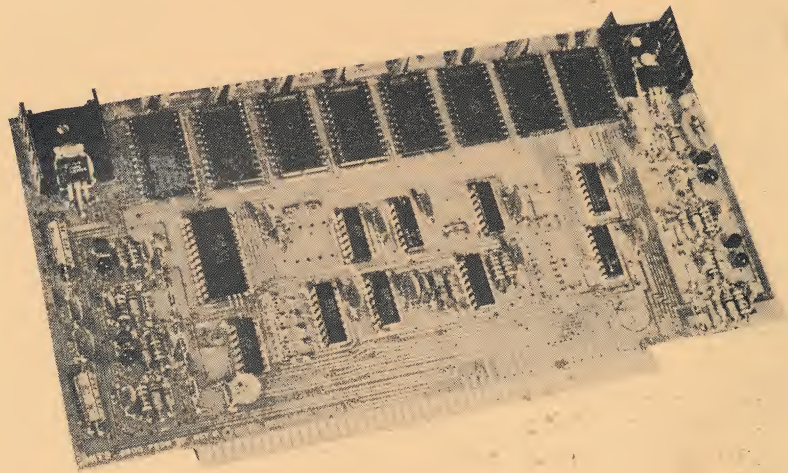
PROMs are electrically programmable and erasable (via ultra-violet light) so that they can be reprogrammed if necessary.

The card can be configured with a minimum of 256 bytes and may be expanded in 256 word increments up to 2,048 bytes by adding PROMs.

There are provisions for patching the number of wait states from 0-3, in order to accommodate different speed devices. Generally, PROMs require from 1-3 wait states, depending on the speed of the device used.

Memory Size: 2,048 bytes (max.).

Access Time: .75 microseconds-2 microseconds (depending on device).



Operation

The PROM card is most useful to systems requiring non-volatile read only memory. Such systems occur in dedicated control applications, boot loaders, or other start-up routines.

The PROM card provides the option of power down circuitry, consisting of four drivers that switch the PROMs "on" and "off" in pairs in order to reduce current drain. In the "off" state, the PROMs draw only 15-20% of the current required in the "on" state. Except for overlaps in switching, only two PROMs can be "on" at a time.

The board may be addressed in 2K increments at any starting address between 0 and 63K by patching the starting address via the 5 jumpers included on the board.



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Altair™ C-700 Printer

Technical Information

The C-700 bidirectional matrix printer produces fast, legible hard-copy for a variety of small business uses such as banking or credit operations, medical laboratories (instrument data logging), reservation systems and inventory. The print head moves right and left seeking the nearest margin of the next line of print. This bidirectional printing method greatly increases efficiency by eliminating the need for time-consuming carriage returns.



Printing Method

The C-700 uses a 64-character subset of USASCII and prints an original and four copies in 132 columns of 5 x 7 dot matrix characters (10 char/inch) at a rate of 60 char/sec (26 lines/min). Character width can be adjusted to provide a total of 66 columns of double-width characters. Printed lines are vertically spaced at 6 lines/inch.

LSI Circuit Design

All of the C-700's electronic circuitry is contained on one printed circuit card. Simple maintenance is provided through the use of custom Large Scale Integration (LSI), which minimizes component parts and improves functional reliability.

Hardware

The interface board occupies one slot on the Altair computer bus and connects to the printer with a 40 conductor plug-in flat cable. The printer measures 7" high x 18" deep x 24.5" wide and requires 50 or 60 Hz, 115 or 230 VAC.

Internal and External Controls

The indicator/switch controls consist of: ON/OFF, SELECT/DESELECT and PAPER OUT INDICATOR.

The internal controls include: Auto Motor Control, Paper Runaway Inhibit and Auto Line Feed on carriage return.



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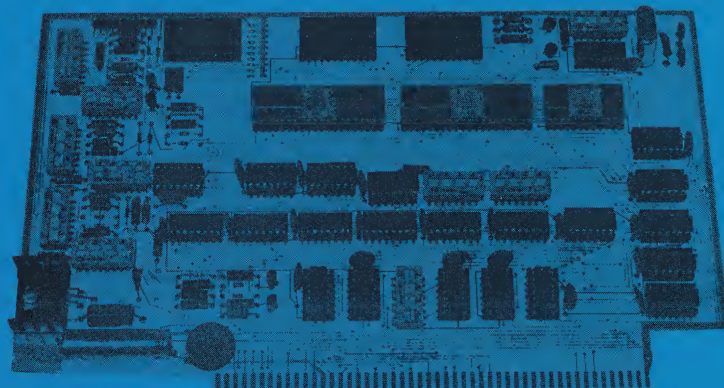
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Altair 680b Universal I/O Card

Technical Information

Expand Your Altair 680b System!

The 680b Universal I/O card greatly enhances the input/output capabilities of the 680b computer by providing (optionally) one serial port and two parallel ports for communication with various terminal devices. Whether you use just one port, two ports or all three at once, each is configured individually and drives an I/O device independently of the other ports. Interface lines are switch selectable for RS-232, TTL and TTY operation.



Parallel Ports

Use the Universal I/O's parallel ports to interface the Altair 680b computer to such devices as a high speed reader and a high speed printer.

Serial Port

Use the Universal I/O's serial port to transmit and receive RS-232 and TTY data through such devices as a CRT, Teletype or Modem. An on-board, crystal-controlled 2.4576 MHz clock allows switch selection of any of the following baud rates: 50, 75, 110, 134.5, 150, 200, 300, 600, 1200, 1800, 2400, 9400 or 9600.

Port Design

The parallel port's design is based upon a Peripheral Interface Adaptor (PIA) which contains all of the Control and Data Registers, thus making most options, such as data direction and interrupt/control structure, software selectable.

The design of the serial port is based upon an Asynchronous Communications Interface Adapter (ACIA) which contains both Control and Status Registers.

Hardware

The serial port plugs into an on-board 10-pin connector with a 12 conductor round cable. Each parallel port plugs into an on-board 24-pin connector with a flat cable. The UI/O occupies one slot on the 680b Expander Card. Power requirements are as follows:

For TTY: + 16v and - 16v max., approx. 63 mA
min., approx. 45 mA

For RS-232: + 16v approx. 36 mA
- 16v 0 mA

Fully expanded: + 5v at approx. 350 mA



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Capabilities

Each PIA contains two sections. Sections A and B each contain two channels: a Control/Status Channel and a Data/Data Direction Channel. Address lines A0 and A1 enable the selection of each Section (A or B) and the Control/Status Channel or the Data Channel of that Section.

The Universal I/O with only one PIA parallel port can handle two inputs (such as a paper tape reader and keyboard) or two output devices (such as a paper tape punch and printer) or any combination of custom applications. A Universal I/O with two PIA parallel ports has 32 data lines (each group of eight is individually selectable). All data lines are fully TTL compatible. Eight of the 16 lines (per PIA parallel port) are capable of directly driving the base of a transistor switch (1.5v at 1 ma).

The ACIA contains both Control and Status Registers. The five control lines allow maximum utilization of sophisticated terminals. These control lines are: transmit data, receive data, data carrier detect, clear to send and request to send. The 8-bit Status Register allows for greater control and handshaking ability by indicating received data available, transmitter buffer empty, carrier detect, clear to send, framing error, received data overflow, parity error, and interrupt request.

All of the input/output lines to or from the ACIA are switch-selectable for RS-232, TTL levels or 20 milliamp current loop (TTY). An on-board, crystal-controlled clock allows user selection for any of 13 baud rates by positioning a dip switch. The Selectable Baud rates are:

50	200	1800
75	300	2400
110	600	4800
134.5	1200	9600
150		

The serial port is software programmable for nine or ten bit transmission as follows:

- 7 data bits + parity bit (odd, even, or none) + 1 or 2 stop bits;
- 8 data bits + 1 or 2 stop bits;
- 8 data bits + 1 stop bit + parity bit (odd or even).



16K Static Memory Card (680b-BSM)

The 680b-BSM 16K memory card consists of four 4096 x 8 bit static memory arrays, an Address Select circuit, a Read/Write circuit, and three voltage regulators.

Hardware

A DIP switch is used for address selection (no address jumpers).

Test points have been installed at important signal outputs for ease of checkout and troubleshooting.

Ferrite beads are used on all common supply lines for noise isolation.

Epoxy solder masks cover areas not to be soldered.

Sockets are provided for all ICs.

Power: + 16V (130 milliamps, maximum)

- 16V (110 milliamps, maximum)

+ 9V (150 milliamps, maximum)

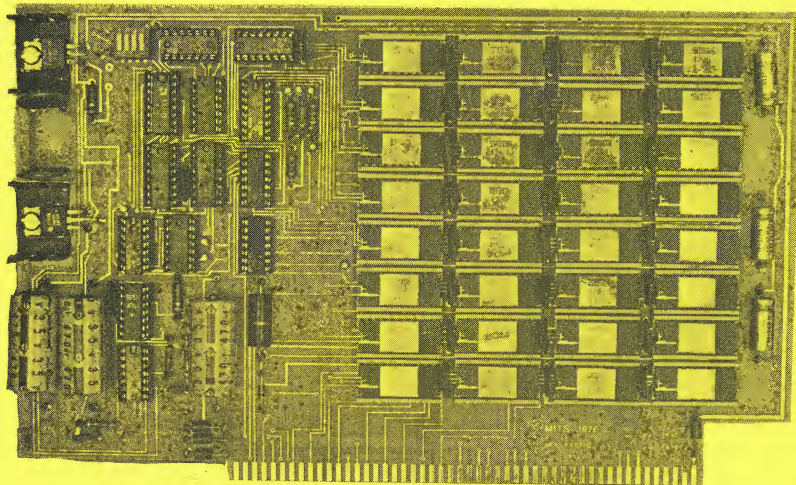
Capabilities

Power consumption of 5 watts or 38 microwatts per bit. This allows operation of two 16K cards without adding a second power transformer.

RAM Access Time: 215 ns., max.

RAM Cycle Time: 400 ns., min.

Up to three 680b-BSM 16K memory cards may be used with the Altair 680b.



Operation

The 680b-BSM memory card operates by retaining data in its memory cells, each cell having a unique location, or address. To place information in a memory cell, the CPU (Motorola 6800) performs a write function, usually caused by a store instruction. Data may also be written into memory by halting the CPU (Halt switch), selecting the memory address (switches A0-A15), selecting the data to be deposited (switches D0-D7), and toggling the deposit switch.

To read data from memory, the CPU must perform a read data operation. This may be done several ways. First, during normal execution of a program, the CPU must fetch (read) instructions and data from memory. Also, the CPU may be instructed to transfer data from memory to some other location, thus requiring a read operation.

Technical Information

Serial Interface Board (88-2SIO)

The 88-2SIO Board design is based upon an Asynchronous Communications Interface Adaptor (ACIA). The ACIA contains both the control register and the status register, so that most options are software selectable.

Hardware

Level Selection: Wire jumpers.

Baud Rate Generator: Crystal-controlled CMOS divider/low power multiplexer.

Device Connection: 12 conductor cable:
10-pin removable connector on board
25-pin connector on back panel

Altair slots: One

Power:

- +5V at 520 milliamps
- +15V at 70 milliamps
- 15V at 70 milliamps

Capabilities

The 88-2SIO board has two serial input/output ports. Each port provides 5 control lines, allowing maximum utilization of sophisticated terminals.

The five control lines are:

- Transmit Data
- Receive Data
- Data Carrier Detect
- Clear to Send
- Request to Send

All lines are user selectable for $\pm 12V$ levels (RS-232), TTL levels (0-5V), or 20 milliamp current loop (Teletype).

Each port is programmable for 9 or 10 bit transmission as follows:

- 7 data bits + parity bit (odd, even, or none) + 1 or 2 stop bits;
- 8 data bits + 1 or 2 stop bits;
- 8 data bits + 1 stop bit + parity bit (odd or even).

Full 8-bit Status Register provides:

- Received Data Available
- Transmitter Buffer Empty
- Carrier Detect
- Clear to Send
- Framing Error
- Received Data Overflow
- Parity Error
- Interrupt Request

The 8-bit status register allows for greater control and handshaking ability.

2SIO transmit and receive interrupts enable/disable is via software control.



Provides an on-board, crystal-controlled clock for any of 8 baud rates (with a single jumper):

- 110
- 150
- 300
- 1200
- 1800
- 2400
- 4800
- 9600

A programmable counter can provide other baud rates:

- 37.5
- 75
- 600

2SIO, with 2 ports, can interface 2 serial I/O devices, each running at a different baud rate and each using a different electrical interconnect. Thus, 2 ports can be operating entirely independently of each other (such as an RS-232 CRT terminal running at 9600 baud and a 20 milliamp Teletype running at 110 baud). 5 volt power consumption is typically 520 milliamps.

Interface levels: TTL, RS-232, TTY.

Bit Configuration: Software selectable for 7 or 8 bits, 1 or 2 stop bits, odd or even parity.



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